ABSTRACT OF THE DISCLOSURE

A processor architecture is provided that supports the decoupling of parameters typically associated with branch/jump instructions. Jump instructions are provided that do not contain an explicit destination address and other jump instructions are provided that do not contain an explicit test condition. In accordance with this invention, the processing system provides a "default" value to any control element in the processor that is not expressly controlled by a particular instruction. In the case of a branch or call instruction, the default destination-address provided to effect the branch or call is the destination-address provided by a prior instruction. Subsequent or alternative branch or call instructions branch to this same address until the default address is set to a different address. In like manner, in most cases, the default condition that is used to determine the result of a conditional test, such as a conditional branch, call, or return instruction, is the last condition specified in a prior instruction. To further support the above objects of this invention, and others, condition-testing can also be effected prior to the execution of conditional instructions.